

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,212,777	May 18, 1993	Gove et al.			
	5,659,785	August 19, 1997	Pechanek et al.			
	6,298,396	October 2, 2001	Loyer et al.			
	6,434,672	August 13, 2002	Gaither			
	6,512,804	January 28, 2003	Johnson et al.			
	6,606,704	August 12, 2003	Adiletta et al.			
	2004/0039880	February 26, 2004	Pentkovski et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "2. TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices," Altera Corporation, July 2005, 28 pages.
	Altera, "APEX II Programmable Logic Device Family," Altera Corporation Data Sheet, August 2002, Ver. 3.0, 99 pages.
	"BlueGene/L – Hardware Architecture Overview," BlueGene/L design team, IBM Research, October 17, 2003 slide presentation, pp. 1-23.
	"BlueGene/L: the next generation of scalable supercomputer," Kissel et al., Lawrence Livermore National Laboratory, Livermore, California, November 18, 2002, 29 pages.
	BlueGene Project Update, January 2002, IBM slide presentation, 20 pages.
	BlueGene/L, "An Overview of the BlueGene/L Supercomputer," The BlueGene/L Team, IBM and Lawrence Livermore National Laboratory, 2002 IEEE. pp. 1-22.
	Epstein, Dave, "IBM Extends DSP Performance with Mfapt," Microprocessor Report, Vol. 9, No. 16 (MicroDesign Resources), December 4, 1995, pp. 1-4 [XL0029013].
	Galanis, M.D. et al., "Accelerating Applications by Mapping Critical Kernels on Coarse-Grain Reconfigurable Hardware in Hybrid Systems," Proceedings of the 13 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 2005, 2 pages.
	Guo, Z. et al., "A Compiler Intermediate Representation for Reconfigurable Fabrics," University of California, Riverside, Dept. of Electrical Engineering, IEEE 2006, 4 pages.
	Gwennap, Linley, "P6 Underscores Intel's Lead," Microprocessor Report, Vol. 9., No. 2, February 16, 1995 (MicroDesign Resources), p. 1 and pp. 6-15.
	Gwennap, Linley, "Intel's P6 Bus Designed for Multiprocessing," Microprocessor Report, Vol. 9, No. 7 (MicroDesign Resources), May 30, 1995, p.1 and pp. 6-10.
	Intel, "Pentium Pro Family Developer's Manual , Volume 3: Operating System Writer's Guide," Intel Corporation, December 1995, [submitted in 4 PDF files: Part I, Part II, Part III and Part IV], 458 pages.
EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.